

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,982,905 B2
APPLICATION NO. : 10/682585
DATED : January 3, 2006
INVENTOR(S) : Dzung H. Nguyen

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7

Line 16, replace "biasing wordlines to unselected cells in the column at a voltage substantially equal to 4.5V and a wordline to the selected cell at a voltage substantially equal to 0V." with --a NAND memory array having columns of cells coupled in series, each cell selected by a wordline;
a select gate source line coupled to a source control transistor at a source end of the column of cells, the select gate source line capable of turning on the source control transistor prior to a drain control transistor when a selected cell is within a predetermined number of cells of the source control transistor; and
a select gate drain line coupled to a drain control transistor at a drain end of the column of cells, the select gate drain line capable of turning on the drain control transistor prior to the source control transistor when the selected cell is within a predetermined number of cells of the drain control transistor.--

Column 7,

Line 40, replace "control transistor, biasing wordlines to unselected cells in the column at a voltage substantially equal to 4.5V and a wordline to the selected cell at a voltage substantially equal to 0V." with --control transistor.--

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,982,905 B2
APPLICATION NO. : 10/682585
DATED : January 3, 2006
INVENTOR(S) : Dzung H. Nguyen

Page 2 of 2

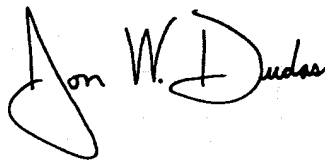
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8,

Line 36, replace "a NAND memory array having columns of cells coupled in series, each cell selected by a wordline; a select gate source line coupled to a source control transistor at a source end of the column of cells, the select gate source line capable of turning on the the source control transistor prior to a drain control transistor when a selected cell is within a predetermined number of cells of the source control transistor; and a select gate drain line coupled to a drain control transistor at a drain end of the column of cells, the select gate drain line capable of turning on the drain control transistor prior to the source control transistor when the selected cell is within a predetermined number of cells of the drain control transistor" with --biasing wordlines to unselected cells in the column at a voltage substantially equal to 4.5V and a wordline to the selected cell at a voltage substantially equal to 0V.

Signed and Sealed this

Fifteenth Day of August, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS

Director of the United States Patent and Trademark Office